Computing Students Talks

26th January 2011

The Good, the Bad and the Unknown

Synthesis of Timing Parameters in Concurrent Systems

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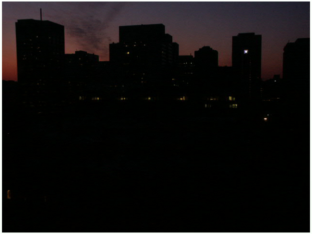
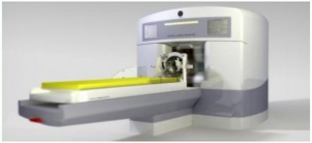
Verification of Real Time Systems

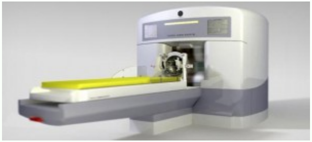
- Motivation





Context: Model Checking Timed Systems (1/2)

- Input



A timed concurrent system

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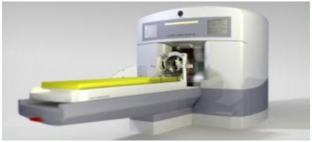

A timed concurrent system

A good behavior expected for the system

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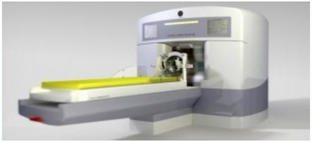


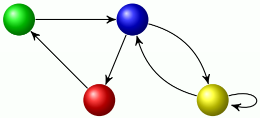
A timed concurrent system

A good behavior expected for the system

- Question: does the system always behave well?

Context: Model Checking Timed Systems (2/2)

- Use of formal methods



$\mathsf{AG}\neg \mathit{bad}$

A finite model of the system

A formula to be satisfied

Context: Model Checking Timed Systems (2/2)

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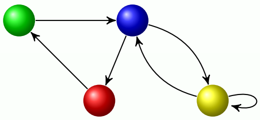

$\overset{?}{\models}$

$AG\neg bad$

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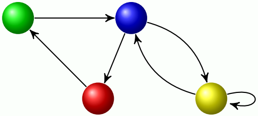


$\models^{?}$ $\quad$ $AG\neg bad$

A finite model of the system $\qquad$ A formula to be satisfied

- Question: does the model of the system satisfy the formula?

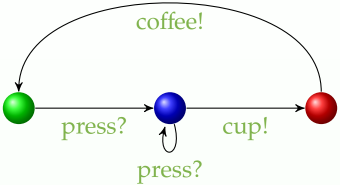
Yes $\qquad$ **No**

Counterexample

Outline

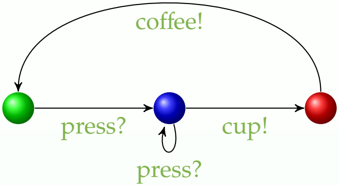
Outline

Model



- Waiting
- Adding sugar
- Delivering coffee

Model



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  - Coffee with no sugar

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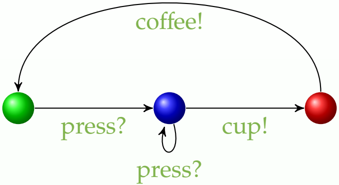

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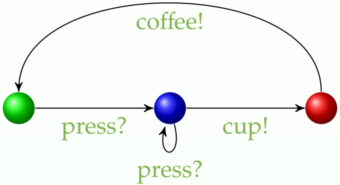

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  - And so on

Temporal Logics

- Specify properties on the order between events
- Example: CTL (Computation Tree Logic) [Clarke and Emerson, 1982]
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Timed Automaton

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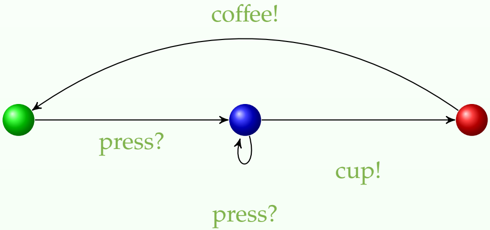
- Finite state automaton (sets of locations and actions)



Timed Automaton

- Finite state automaton (sets of locations and actions) augmented with a set X of clocks [Alur and Dill, 1994]
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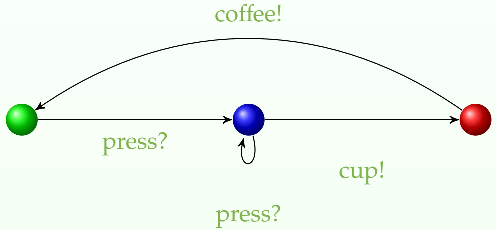

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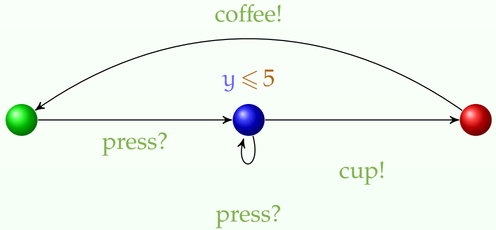

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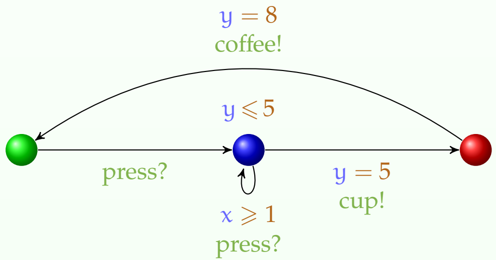

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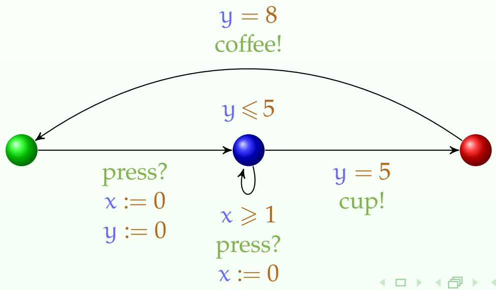
  - Clock reset: some of the clocks can be set to 0 at each transition



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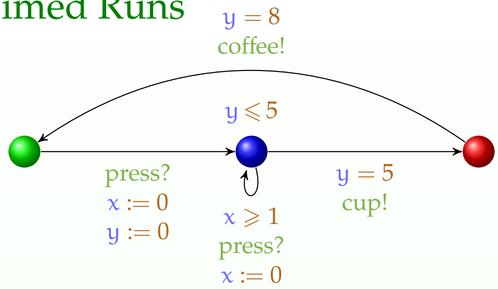

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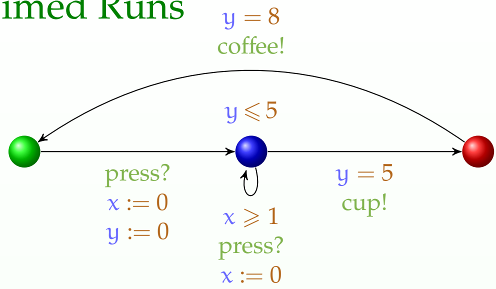

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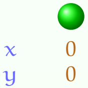

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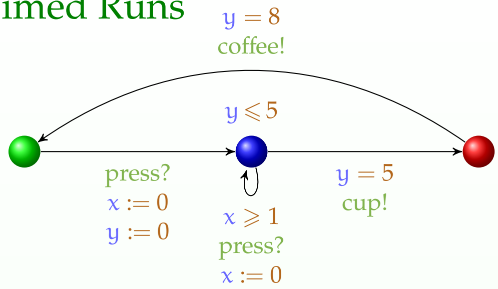

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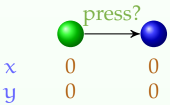

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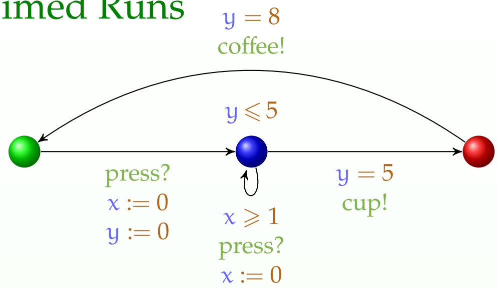

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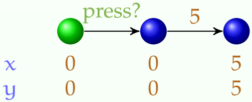

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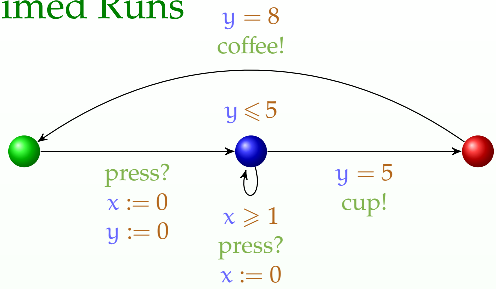

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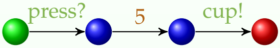

x	0	0	5	5
y	0	0	5	5

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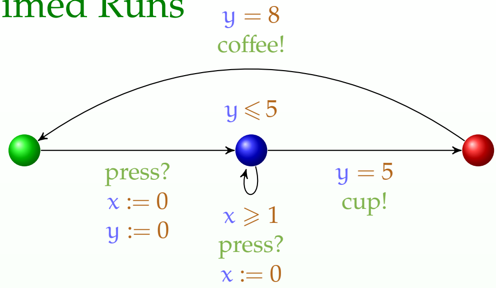

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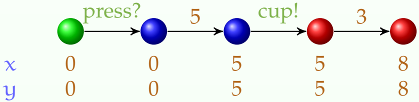

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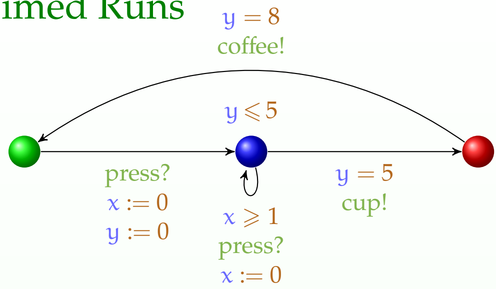

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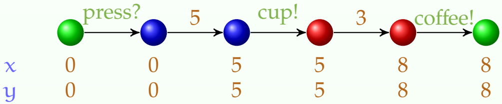

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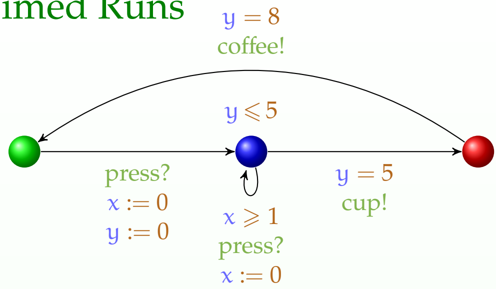

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		press?		5		cup!		3		coffee!	
x	0		0		5		5		8		8
y	0		0		5		5		8		8

  - Coffee with 2 doses of sugar

x	0
y	0

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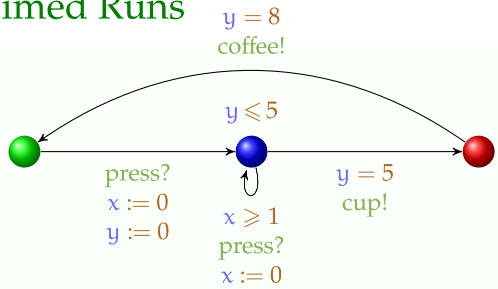

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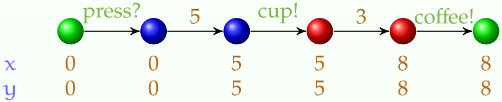

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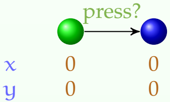

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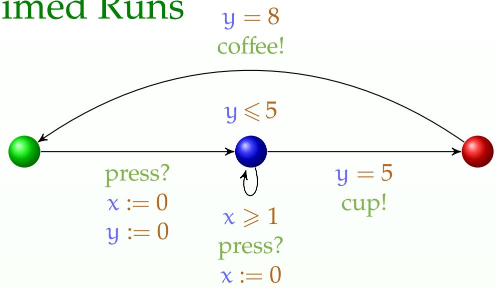

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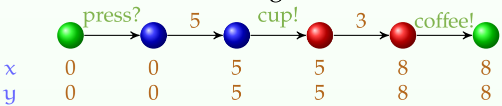

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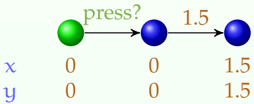

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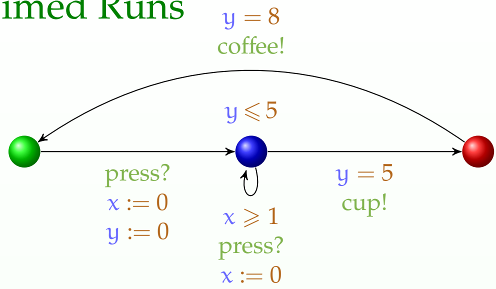

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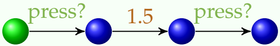

x	0	0	1.5	0
y	0	0	1.5	1.5

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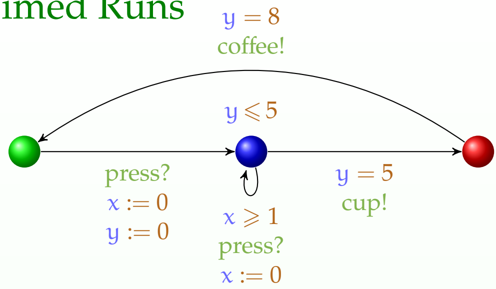

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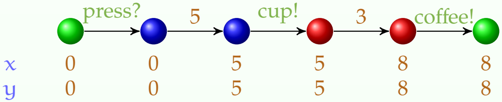

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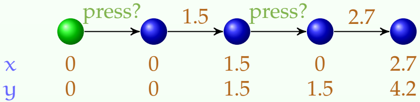

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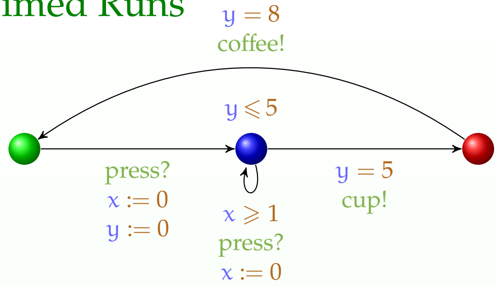

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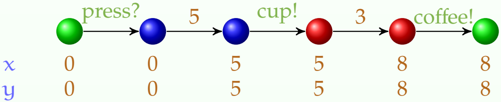

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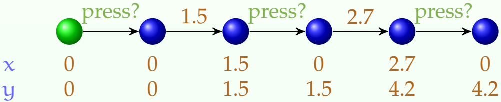

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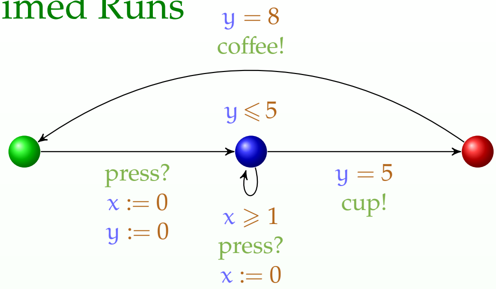

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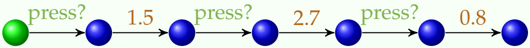
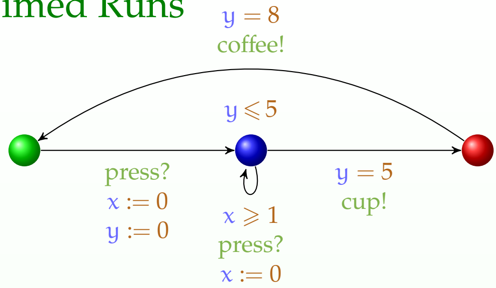


x	0	0	1.5	0	2.7	0	0.8
y	0	0	1.5	1.5	4.2	4.2	5

Timed Runs



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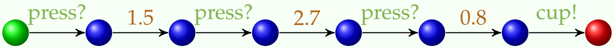

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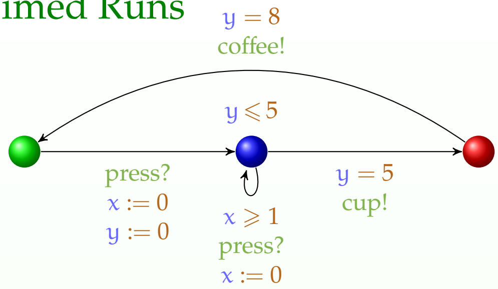

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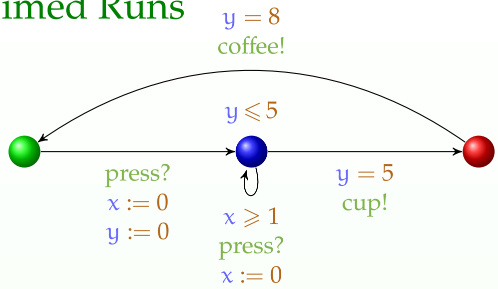

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Dense Time

- Time is dense: transitions can be taken anytime
  - Infinite number of timed runs
  - Model checking needs a finite structure!
- Some runs are equivalent
  - Taking the press? action at $t = 1.5$ or $t = 1.57$ is equivalent w.r.t. the possible actions
- Idea: reason with abstractions
  - Region automaton [Alur and Dill, 1994]
  - Example: in location , all clock values in the following region are equivalent

$$x \geqslant 1 \land y \leqslant 5 \land x = y$$

  - This abstraction is finite

Timed Temporal Logics

- Specify properties on the order and the delay between events
- Example: TCTL (Timed CTL) [Alur et al., 1993a]
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  - "After the first time the button is pressed, a coffee is always eventually delivered within 10 units of time." ($\surd$)
  - "It must never happen that the button can be pressed twice within 1 unit of time." ($\times$)
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Timed Temporal Logics

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Towards a Parametrization...

- Interesting problems
  - Robustness
    - Does the system still behave the same if one of the delays (slightly) changes?
  - Optimization of timing constants
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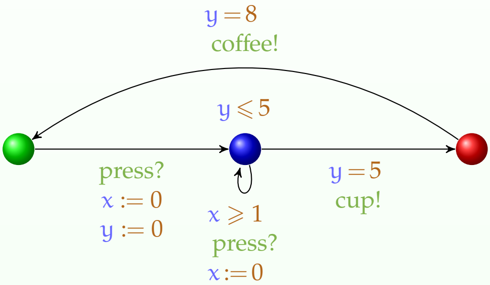
- Idea: reason with parameters (unknown constants)

Outline

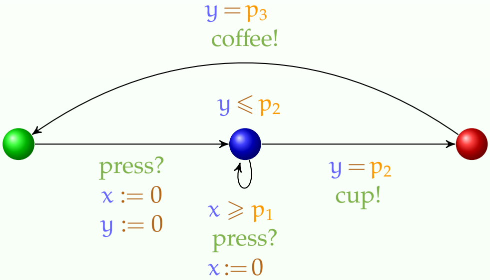
Parametric Timed Automaton

- Timed automaton (sets of locations, actions and clocks)



Parametric Timed Automaton

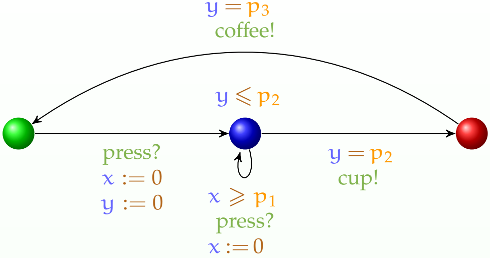
- Timed automaton (sets of locations, actions and clocks) augmented with a set P of parameters [Alur et al., 1993b]
  - Unknown constants used in guards and invariants

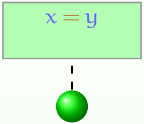


Symbolic Exploration

- Iterative exploration of symbolic states
  - Symbolic state: location and constraint on the clocks and parameters

Symbolic Exploration: Coffee Machine





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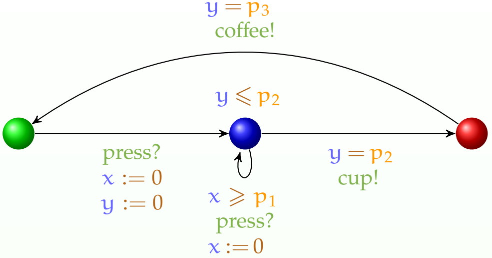

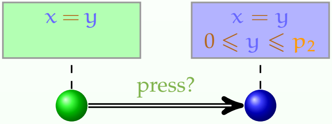

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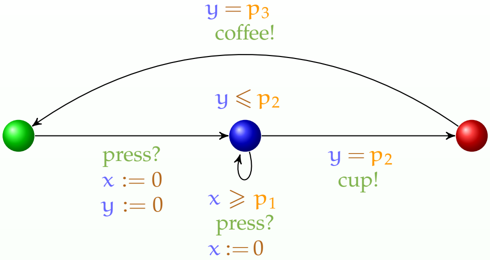

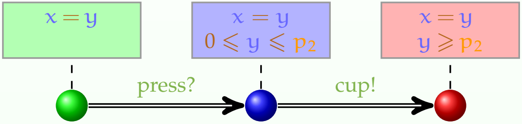

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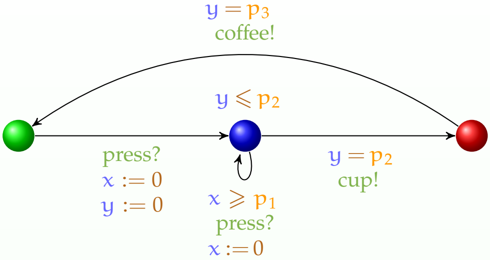

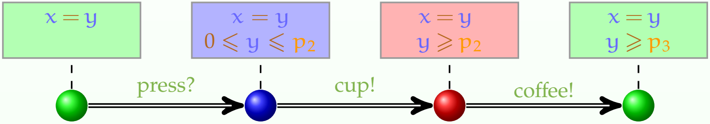

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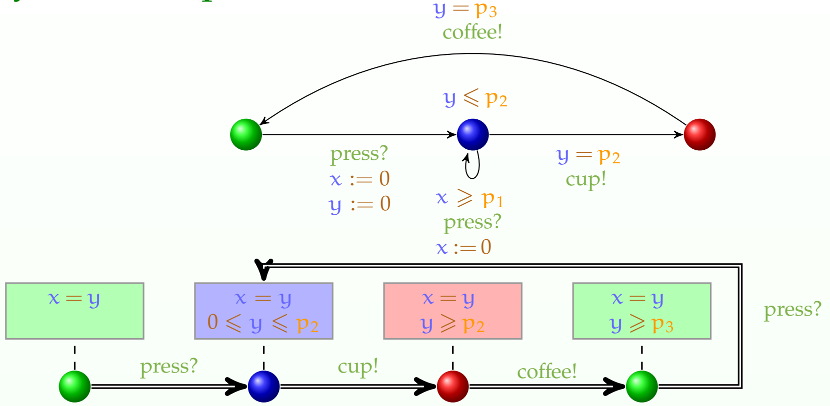

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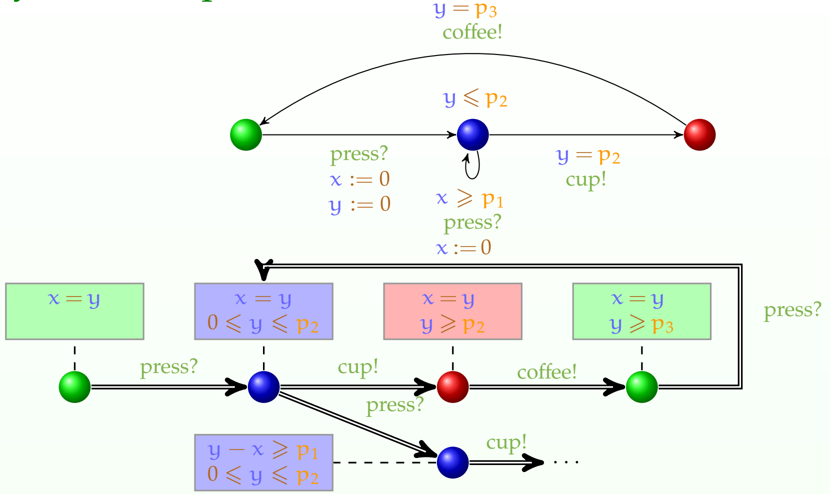

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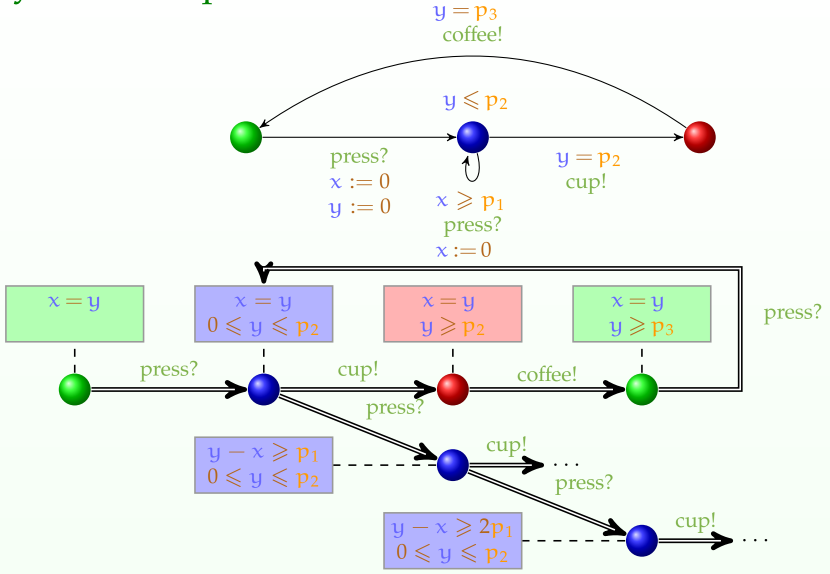

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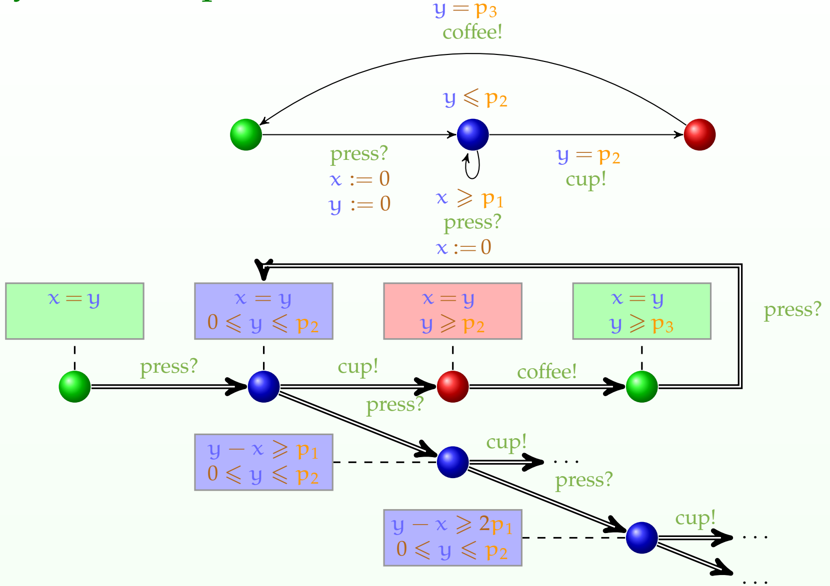

Undecidability

- The symbolic exploration is infinite in general
- No possible abstraction like for Timed Automata

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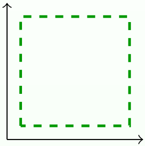
Bad News

(Almost) all interesting problems are undecidable for Parametric Timed Automata.

Outline

Synthesis of Parameters (1/2)

- The good parameters problem
  - "Given a bounded parameter domain, find a set of parameter valuations of good behavior"



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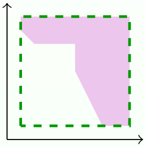

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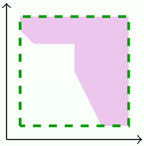

- Interesting problem

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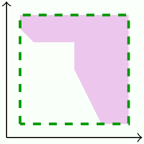


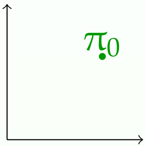
- Interesting problem
  - But undecidable!

Synthesis of Parameters (2/2)

- Possible options to deal with undecidability
  - Semi algorithms
    - Example: Computation of all the reachable states, and intersection with the bad states [Henzinger and Wong-Toi, 1996]
  - Approximations
    - Example: Use of octahedra [Clarisó and Cortadella, 2007]
  - Restrictions to decidable subclasses
    - Example: L/U automata [Hune et al., 2002]

An Inverse Method for PTAs

- Original method for synthesis of parameters [André et al., 2009]
  - "Given a reference parameter valuation π_0, find other valuations around π_0 of same (linear-time) behavior"



Input

$p_1 = 1$

$p_2 = 5$

$p_3 = 8$

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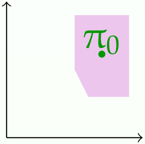

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$p_3 \geqslant p_2$
$\wedge\ 6p_1 > p_2$
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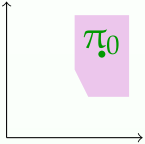

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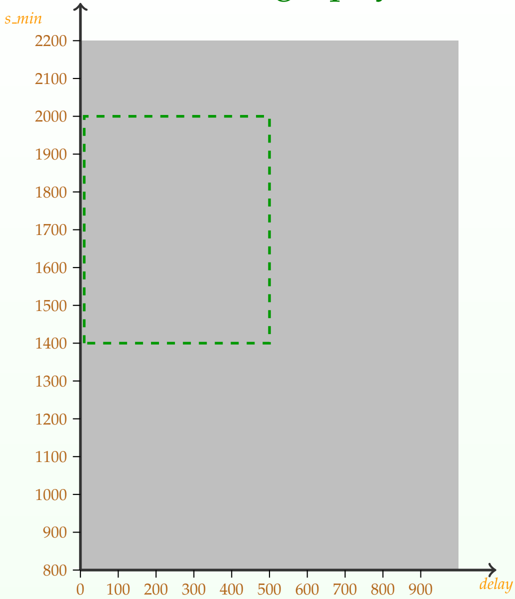
$\wedge\ p_2 \geqslant 5p_1$

- Properties
  - Semi-algorithm
  - Not complete
- Advantages
  - Exact method
  - Behaves well in practice!

Behavioral Cartography of Timed Automata (1/2)



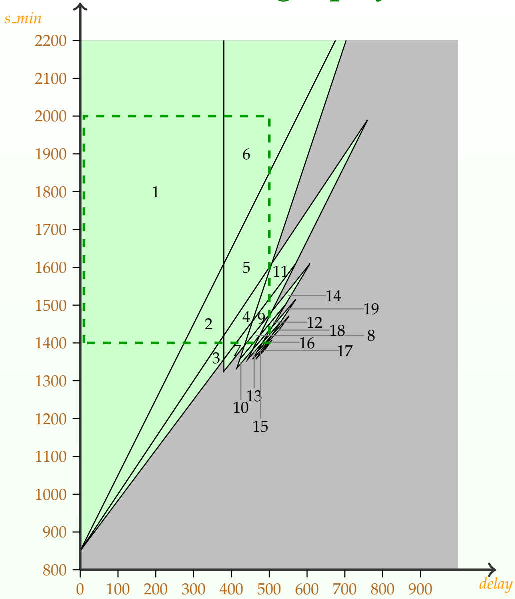
- Idea: repeatedly call the inverse method [André and Fribourg, 2010]

  ⇝ Cover the parametric space with tiles

  - Parametric zones with uniform behavior

Example: Root Contention Protocol

Behavioral Cartography of Timed Automata (1/2)



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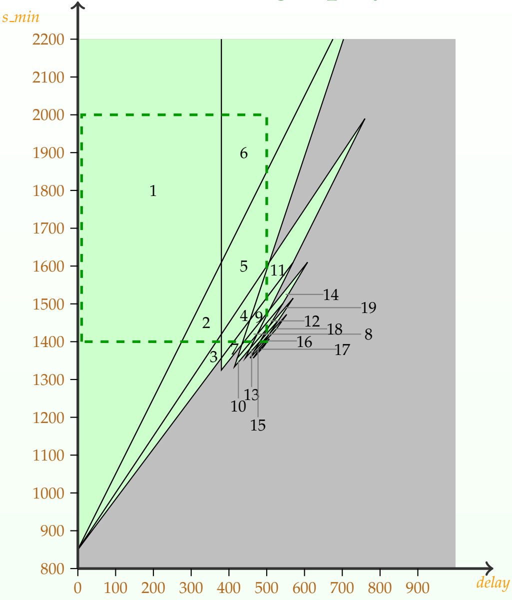

- Idea: repeatedly call the inverse method [André and Fribourg, 2010]

  ⇝ Cover the parametric space with tiles

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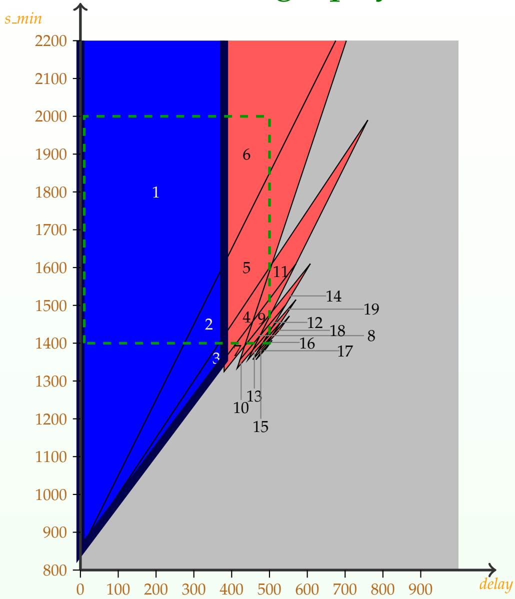
- Remarks
  - Tiles may be infinite
  - The cartography may not cover the whole real-valued space

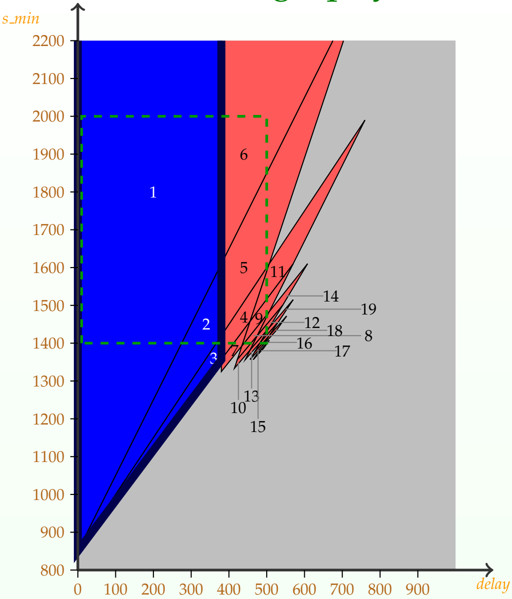
Example: Root Contention Protocol

Behavioral Cartography of Timed Automata (2/2)



- Partition into good and bad subspaces
  - Good if the property is true
  - Bad if the property is false
  - Unknown if not covered by any tile

Behavioral Cartography of Timed Automata (2/2)



- Partition into good and bad subspaces
  - Good if the property is true
  - Bad if the property is false
  - Unknown if not covered by any tile
- Advantages
  - Independent of the property (Only the partition depends on the property)
  - Covers much of the parametric space in practice

Summary

- Synthesis of parameters for real-time concurrent systems important
  - Robustness
  - Optimization of timing constants
  - Avoidance of numerous verifications
- Undecidable in the general case
  - Possible solutions
    - Semi algorithms
    - Approximations
    - Restrictions to decidable subclasses
- Still ongoing work!

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Summary of Experiments: *IM*

- Computation times of various case studies
  - Experiments conducted on an Intel Core2 Duo 2.4 GHz with 2 Gb

Example	PTAs	loc./PTA	$\lvert X \rvert$	$\lvert P \rvert$	iter.	$\lvert K_0 \rvert$	states	trans.	Time
SR-latch	3	[3, 8]	3	3	5	2	4	3	0.007
Flip-flop	5	[4, 16]	5	12	9	6	11	10	0.122
And–Or	3	[4, 8]	4	12	14	4	13	13	0.15
Latch circuit	7	[2, 5]	8	13	12	6	18	17	0.345
CSMA/CD	3	[3, 8]	3	3	19	2	219	342	1.01
RCP	5	[6, 11]	6	5	20	2	327	518	2.3
BRP	6	[2, 6]	7	6	30	7	429	474	34
SIMOP	5	[5, 16]	8	7	53	9	1108	1404	67
SPSMALL	28	[2, 11]	28	62	94	45	129	173	461

Summary of Experiments: *BC*

- Computation time for the cartography algorithm
  - Experiments conducted on an Intel Core2 Duo 2.4 GHz with 2 Gb

Example	PTAs	loc./PTA	$\|X\|$	$\|P\|$	$\|V_0\|$	tiles	states	trans.	Time (s)
SR-latch	3	$[3, 8]$	3	3	1331	6	5	4	0.3
Flip-flop	5	$[4, 16]$	5	2	644	8	15	14	3
Latch circuit	7	$[2, 5]$	8	4	73062	5	21	20	96.3
And–Or	3	$[4, 8]$	4	6	75600	4	64	72	118
CSMA/CD	3	$[3, 8]$	3	3	2000	140	349	545	269
RCP	5	$[6, 11]$	6	3	186050	19	5688	9312	7018
SPSMALL	28	$[2, 11]$	28	3	784	213	145	196	31641